WHAT IS CLAIMED IS:

1. A semiconductor element, comprising:

a first base layer of a first conductivity type;

a second base layer of a second conductivity type formed selectively in one surface region of said first base layer;

an emitter layer or a source layer of the first conductivity type formed selectively in a surface region of said second base layer;

a gate electrode formed on that portion of said second base layer which is positioned between said emitter layer or source layer and said first base layer with a gate insulating film interposed between said gate electrode and said second base layer;

a collector layer or a drain layer formed on the other surface region of said first base layer or formed selectively on one surface region of the first base layer;

a first main electrode formed on said collector layer or on said drain layer;

a second main electrode formed on said emitter layer or source layer and on said second base layer; and

a channel region formed in contact with said gate insulating film to permit the carrier to migrate between the emitter layer or source layer and the first base layer, said channel region having an impurity

concentration profile such that the impurity concentration that permits bringing about a pinch-off phenomenon most promptly within said channel is formed in a position closer to the first base layer than to the junction between the emitter layer or source layer and the second base layer.

2. The semiconductor element according to claim 1, wherein the impurity concentration causing said pinch-off phenomenon in a position close to said first base layer is equal to the highest concentration in said impurity concentration profile of said channel region.

3. The semiconductor element according to claim 1, wherein the impurity concentration profile in said channel region has, in a region between the junction portion with said emitter layer or source layer and a point of the highest impurity concentration, an impurity concentration gradient lower than that in said junction portion, the impurity concentration gradient in said junction portion being formed by the overlapping of the impurity concentration profile in said second base layer with the impurity concentration profile in said emitter layer or source layer.

4. The semiconductor element according to claim 1, wherein, in said channel region, the channel conductance between said first base layer and a point of the highest impurity concentration in said second base layer is higher than the channel conductance

between said emitter layer or source layer and a point of the highest impurity concentration in said second base layer.

5. The semiconductor element according to claim 1, wherein said gate electrode is buried in a trench with a gate insulating film interposed between said gate electrode and said trench, said trench being formed to extend from the surface of said emitter layer or source layer to reach an intermediate portion of said first base layer through said second base layer.

6. The semiconductor element according to claim 1, wherein said second main electrode is formed on the bottom surface and/or the side surface of a groove formed to extend downward to reach an intermediate portion of said second base layer.

7. The semiconductor element according to claim 1, wherein said gate electrode is formed on said gate insulating film formed on the surface of said second base layer.

8. A semiconductor element, comprising:

a first base layer of a first conductivity type;

a second base layer of a second conductivity type formed selectively in one surface region of said first base layer;

an emitter layer or a source layer of the first conductivity type formed selectively in a surface region of said second base layer;

a gate electrode formed on that portion of said second base layer which is positioned between said emitter layer or source layer and said first base layer with a gate insulating film interposed between said gate electrode and said second base layer;

a collector layer or a drain layer formed on the other surface region of said first base layer or formed selectively on one surface region of the first base layer;

a first main electrode formed on said collector layer or on said drain layer;

a second main electrode formed on said emitter layer or source layer and on said second base layer; and

a third base layer formed within said second base layer so as to be isolated from said emitter layer or source layer and formed in contact with said gate insulating film, the point of the highest impurity concentration of a first impurity concentration profile along the gate insulating film within said third base layer and in the direction in which said emitter layer or source layer, the second base layer, and the first base layer are arranged in the order mentioned being positioned closer to the first base layer than the point of the highest impurity concentration of a second impurity concentration profile along the gate insulating film within said second base layer and in

the direction in which the emitter layer or source layer, the second base layer and the first base layer are arranged in the order mentioned.

9. The semiconductor element according to claim 8, wherein the highest impurity concentration of said first impurity concentration profile within said third base layer is not lower than the highest impurity concentration of said second impurity concentration profile within said second base layer.

10. The semiconductor element according to claim 8, wherein a third impurity concentration profile, which results from the overlapping of said first and second impurity concentration profiles, has an impurity concentration gradient smaller than the impurity concentration gradient at the junction with said emitter layer or said source layer in the position between said junction and the position of the highest impurity concentration, the impurity concentration gradient in said junction being formed by the overlapping between said second impurity concentration profile and a fourth impurity concentration profile in said emitter layer or source layer.

11. The semiconductor element according to claim 9, wherein, in said second and third base layers, the channel conductance between said first base layer and the point of the highest impurity concentration within said third base layer is higher than the channel

conductance between said emitter layer or source layer and the position of the highest impurity concentration within said third base layer.

12. The semiconductor element according to claim 8, wherein said third base layer is in contact with said first base layer.

13. The semiconductor element according to claim 8, wherein the region of the highest impurity concentration in said third base layer is selectively formed at the interface between said second base layer and said gate insulating film and in the vicinity of said interface.

14. The semiconductor element according to claim 8, wherein said gate electrode is buried in a trench with a gate insulating film interposed between said gate electrode and said trench, said trench being formed to extend from the surface of said emitter layer or source layer to reach an intermediate portion of said first base layer through said second base layer.

15. The semiconductor element according to claim 8, wherein said second main electrode is formed on the bottom surface and/or side surface of a groove formed to extend through said second base layer to reach an intermediate depth of said third base layer and is in contact with said third base layer on the bottom surface and/or the side surface of said groove.

16. The semiconductor element according to claim 8,

wherein said gate electrode is formed on said gate insulating film formed on the surface of said second base layer.

17. A semiconductor element, comprising:

a first base layer of a first conductivity type;

a second base layer of a second conductivity type formed selectively in one surface region of said first base layer;

an emitter layer or a source layer of the first conductivity type formed selectively in a surface region of said second base layer;

a gate electrode formed on that portion of said second base layer which is positioned between said emitter layer or source layer and said first base layer with a gate insulating film interposed between said gate electrode and said second base layer;

a collector layer or a drain layer formed on the other surface region of said first base layer or formed selectively on one surface region of the first base layer;

a first main electrode formed on said collector layer or on said drain layer;

a second main electrode formed on said emitter layer or source layer and on said second base layer; and

a channel region formed in contact with said gate insulating film to permit the carrier to migrate

between said emitter layer or source layer and said first base layer, said channel region having an impurity concentration profile such that the impurity concentration is substantially constant along said gate insulating film and in the direction in which the emitter layer or source layer, the second base layer, and the first base layer are formed in the order mentioned.

18. The semiconductor element according to claim 17, wherein said gate electrode is buried in a trench with a gate insulating film interposed between said gate electrode and said trench, said trench being formed to extend from the surface of said emitter layer or source layer to reach an intermediate portion of said first base layer through said second base layer.

19. The semiconductor element according to claim 17, wherein said gate electrode is formed on said gate insulating film formed on the surface of said second base layer.

20. A method of fabricating a semiconductor element, comprising the steps of:

selectively forming a second base layer of a second conductivity type in one surface region of a first base layer of a first conductivity type, said second base layer having an impurity concentration profile such that the point of the highest impurity concentration is positioned in a region close to the

junction between the second base layer and the first base layer;

selectively forming an emitter layer or source layer of the first conductivity type in a surface region of said second base layer;

forming a gate electrode on the surface of that region of said second base layer which is positioned between said emitter layer or source layer and said first base layer with a gate insulating film interposed between said gate electrode and said second base layer;

selectively forming a collector layer or drain layer in the other surface region of said first base layer or in one surface region of said first base layer; and

forming a first main electrode in contact with said collector layer or drain layer and a second main electrode in contact with said emitter layer or source layer and said second base layer.

21. The method of fabricating a semiconductor element according to claim 20, wherein said step of forming said second base layer includes the sub-steps of:

forming a third base layer of the second conductivity type by selectively implanting ions of an impurity of the second conductivity type into a surface region of said first base layer, followed by thermally diffusing the implanted impurity ions; and

implanting ions of an impurity of the first conductivity type into a surface region of said third base layer, followed by thermally diffusing the implanted impurity ions, thereby lowering the concentration of the impurity of the second conductivity type in the surface region of said third base layer so as to form a fourth base layer of the second conductivity type.

22. The method of fabricating a semiconductor element according to claim 20, wherein said step of forming said second base layer includes the sub-steps of:

selectively implanting ions of an impurity of the second conductivity type into a surface region of said first base layer, followed by thermally diffusing the implanted ions so as to form a third base layer of the second conductivity type; and

applying heat to said third base layer so as to diffuse outward the impurity of the second conductivity type in the vicinity of the surface of said third base layer, thereby lowering the concentration of the impurity of the second conductivity type in the vicinity of the third base layer so as to form a fourth base layer of the second conductivity type.

23. The method of fabricating a semiconductor element according to claim 20, wherein said step of forming said second base layer includes the sub-steps

of:

forming a third base layer of the second conductivity type by implanting ions of an impurity of the second conductivity type into a surface region of said first base layer at a first dose and under a first accelerating energy;

forming a fourth base layer of the second conductivity type in said third base layer, the impurity concentration in said fourth base layer being higher than that in said third base layer, by implanting ions of an impurity of the second conductivity type into said third base layer at a second dose higher than said first dose and under a second accelerating energy higher than said first accelerating energy; and

thermally diffusing the implanted ions of the second conductivity type.

24. The method of fabricating a semiconductor element according to claim 20, wherein said step of forming said gate electrode includes the sub-steps of:

forming a trench extending from the surface of said emitter layer or source layer to reach an intermediate depth of said first base layer through said second base layer;

forming a gate insulating film on the bottom and side wall of said trench; and

burying a gate electrode in said trench.

25. A method of fabricating a semiconductor element, comprising the steps of:

selectively forming a second base layer of a second conductivity type in one surface region of a first base layer of a first conductivity type;

selectively forming an emitter layer or source layer of the first conductivity type in a surface region of said second base layer;

forming a gate electrode on the surface of that region of said second base layer which is positioned between said emitter layer or source layer and said first base layer with a gate insulating film interposed between said gate electrode and said second base layer, and a third base layer of the second conductivity type, which is isolated from said emitter layer or source layer, within said second base layer;

selectively forming a collector layer or drain layer in the other surface region of said first base layer or in one surface region of said first base layer; and

forming a first main electrode in contact with said collector layer or drain layer and a second main electrode in contact with said emitter layer or source layer and said second base layer.

26. The method of fabricating a semiconductor element according to claim 25,

wherein said step of forming said third base layer

includes the sub-steps of:

forming said gate electrode, followed by forming a groove having the bottom positioned within said second base layer; and

implanting ions of an impurity of the second conductivity type into a region in the vicinity of the bottom portion of said groove, followed by thermally diffusing the implanted ions so as to form a third base layer of the second conductivity type at least in contact with said gate insulating film, the position of the highest concentration of the impurity concentration distribution within said third base layer being closer to said first base layer than the position of the highest concentration of the impurity concentration distribution within said second base layer; and

wherein said second main electrode is formed in contact with said second and third base layers and said emitter layer or source layer on the bottom surface and/or side surface of said groove in the step of forming said second main electrode.

27. The method of fabricating a semiconductor element according to claim 25, wherein said step of forming said gate electrode and said third base layer includes the sub-steps of:

forming a trench extending through said emitter layer or source layer to reach said first base layer;

forming a third base layer by implanting ions of

an impurity of the second conductivity type into a region in the vicinity of the bottom of said trench, followed by thermally diffusing said impurity;

deepening said trench to reach an intermediate depth of said first base layer;

forming said gate insulating film on the bottom and side surface of said trench; and

burying said gate electrode in said trench.

28. The method of fabricating a semiconductor element according to claim 26, wherein said step of forming said gate electrode and said third base layer includes the sub-steps of:

forming a trench extending through said emitter layer or source layer and having the bottom positioned within said second base layer;

forming a masking material on the side wall of said trench;

burying a diffusion source containing an impurity of the second conductivity type in said trench;

forming a third base layer of the second conductivity type by applying heat to said diffusion source so as to diffuse the impurity of the second conductivity type contained in said diffusion source into a region in the vicinity of the bottom of said trench;

removing the diffusion source positioned within the trench;

deepening the trench to reach an intermediate depth of said first base layer;

forming a gate insulating film on the bottom and side surface of the trench; and

burying said gate electrode in the trench.

29. The method of fabricating a semiconductor element according to claim 26,

wherein said step of forming said third base layer includes the sub-steps of:

forming a gate electrode, followed by forming a groove having the bottom positioned within said second base layer;

forming a masking material layer on the side wall of said groove;

burying a diffusion source containing an impurity of the second conductivity type in said groove;

forming a third base layer of the second conductivity type by applying heat to said diffusion source so as to diffuse the impurity of the second conductivity type contained in said diffusion source into a region in the vicinity of the bottom of said groove; and

removing said diffusion source positioned within said groove; and

wherein said first main electrode is formed in contact with said second and third base layers and with said emitter layer or source layer on the bottom and/or

side surface of said groove in the step of forming said first main electrode.

30. A method of fabricating a semiconductor element, comprising the steps of:

selectively forming an emitter layer or source layer of a first conductivity type in one surface region of a first base layer of the first conductivity type;

forming a trench extending through said emitter layer or source layer and having the bottom portion positioned within said first base layer;

forming a gate insulating film to cover the bottom and the side surface of said trench;

forming a gate electrode on said gate insulating film;

forming a groove having a bottom positioned within said first base layer;

forming a second base layer of the second conductivity type in a surface region of said first base layer such that said second base layer is in contact with said gate insulating film by introducing an impurity of the second conductivity type into said first base layer in the bottom and in the vicinity of the side wall of said groove, followed by applying a thermal diffusion to the introduced impurity;

forming a third base layer of the second conductivity type within said second base layer such

that said third base layer is in contact with said gate insulating film by introducing an impurity of the second conductivity type into the second base layer in the vicinity of the bottom of said groove, followed by applying a thermal diffusion to the introduced impurity;

selectively forming a collector layer or drain layer in the other surface region of said first base layer; and

forming a first main electrode in contact with said collector layer or drain layer and a second main electrode in contact with said emitter layer or source layer, and said second and third base layers, said second main electrode being in contact with said third base layer in the bottom and/or the side wall of said groove and in contact with said second base layer and said emitter layer or source layer in the side wall of said groove.

31. A method of fabricating a semiconductor element, comprising the steps of:

forming a second base layer of a second conductivity type in one surface region of a first base layer of a first conductivity type such that the impurity concentration is constant in the depth direction of said second base layer;

selectively forming an emitter layer or source layer of the first conductivity type in a surface

region of said second base layer;

forming a gate electrode on the surface of that region of said second base layer which is positioned between said emitter layer or source layer and said first base layer with a gate insulating film interposed between said gate electrode and said second base layer;

selectively forming a collector layer or drain layer on the other surface region of said first base layer or on one surface region of said first base layer; and

forming a first main electrode in contact with said collector layer or drain layer and a second main electrode in contact with said emitter layer or drain layer and said second base layer.

32. The method of fabricating a semiconductor element according to claim 31,

wherein said step of forming said second base layer includes the sub-steps of:

forming a third base layer of the second conductivity type on said first base layer such that the impurity concentration in the depth direction is set constant at a first concentration; and

forming a fourth base layer of the second conductivity type on said third base layer such that the impurity concentration in the depth direction is set constant at a second concentration higher than said first concentration; and

wherein said emitter layer or source layer is formed in said fourth base layer.